## DEPARTMENT OF ELECTRICAL ENGINEERING INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR, HOWRAH-711 103.

No. 172/2020/EE-3/21(KM-PEL)

Dated: 28/02/2020

From: The Head of the Department, Electrical Engineering,

IIEST, Shibpur, Howrah-711 103

To: Enlisted vendors of the institute and other interested parties/ For Website Tender.

Dear Sir(s),

Sealed quotations are invited for supply of the following item(s) within 12/03/2020. The quotation should include the taxes as per rule, delivery charges, entry tax if any, etc. to Indian Institute of Engineering Science and Technology, Shibpur and should mention a firm delivery period. Preferences will be given to the suppliers who can supply ex-stock.

The vendors, who are not enlisted in the Institute register, should submit the copies of their valid Trade License, PAN, latest Income Tax / Sales Tax Statement /Return, SSI/MSME certificate, GST certificate if any etc. and any other commercial credentials.

Yours faithfully,

Signature of the indenting Officer/ Concerned Faculty Member

28/02/2020

Prof. & Head of EE Dept. IIEST, Shibpur, Howrah – 711 103

Prasid Syam

List of Items: FPGA kits required for Power Electronics laboratory, IIESTar Shippurotes 2 sets (quantity is tentative, final quantity to depend on funds available, quote to be provided based on per unit basis)

<u>Required Specifications:</u> Each FPGA kit set should have the following features/specifications:

ALTERA-based/equivalent Field Programmable Gates Array (FPGA) processor chip integrated properly with requisite power supply, Analog-to-Digital Converter (ADC's), Digital-to-analog Converters (DAC's), buffers, driver, interface card etc. The total solution has to be confined within preferably one PCB or in two PCB's at most. Design should be compact, modular and such that EMI problems are negligible. The kit must provide the following:

- (i) Minimum 8 no.s of ADC channels (maximum 1.6 μs conversion time per channel), minimum 4 numbers of DAC channels
- (ii) 60 Input/Output (I/O) lines minimum
- (iii) 12k logic elements minimum
- (iv) Serial programming option, JTAG equivalent byteblaster cable (USB computer port compatible) should accompany the kit
- (v) RS232 interface, USB interface, LCD interface, CAN interface features
- (vi) In-built 64 kB serial EEPROM memory
- (vii) Minimum 4 MB flash memory (active serial configuration device)
- (viii) PLL options to be present
- (ix) The kit should be programmable by using ALTERA's open source programming/debugging software, freely available in internet

User/Customer will connect the board/kit to a 230V, 50 Hz single phase AC mains and all internal power supplies, viz. +/- 15V, +/-5V etc. as applicable for the kit, should be derived as per internal design of vendor and the internal SMPS/linear power supplies must be provided by the vendor.

Input output pins and/or connectors for power supplies, JTAG connection, digital I/O's, analog ADC inputs, analog DAC output, analog ground, digital ground should be available on the PCB (s). A proper work manual, instruction manual should be supplied while delivering the items where all explanations, PCB schematics, I/O addresses, pinout diagrams, pin decoding etc. should be clearly mentioned which will be utilized to program the kit properly. Final acceptance and subsequent payment will be made to the vendor after satisfactory testing at customer's premises and after demonstration.

A minimum of two years' warranty has to be provided.